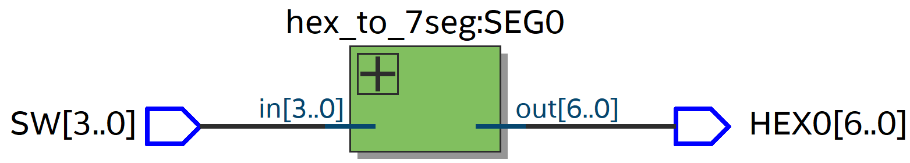
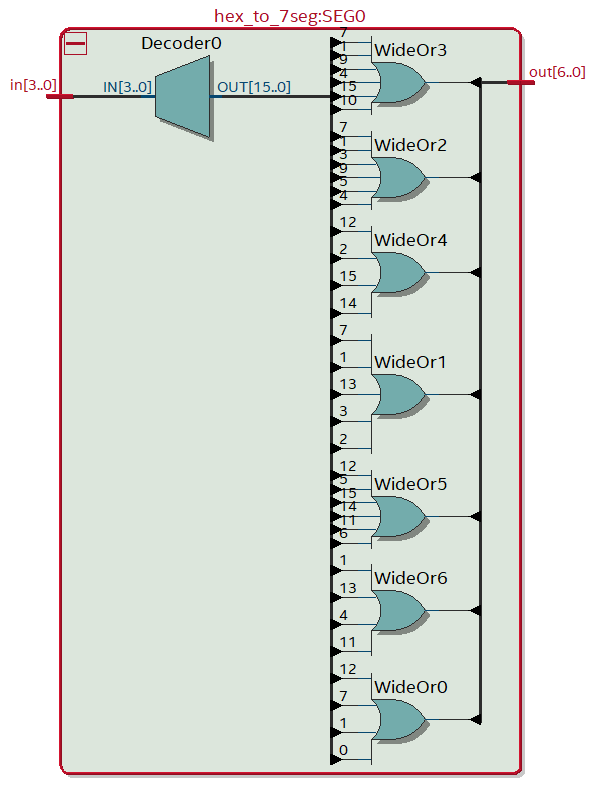
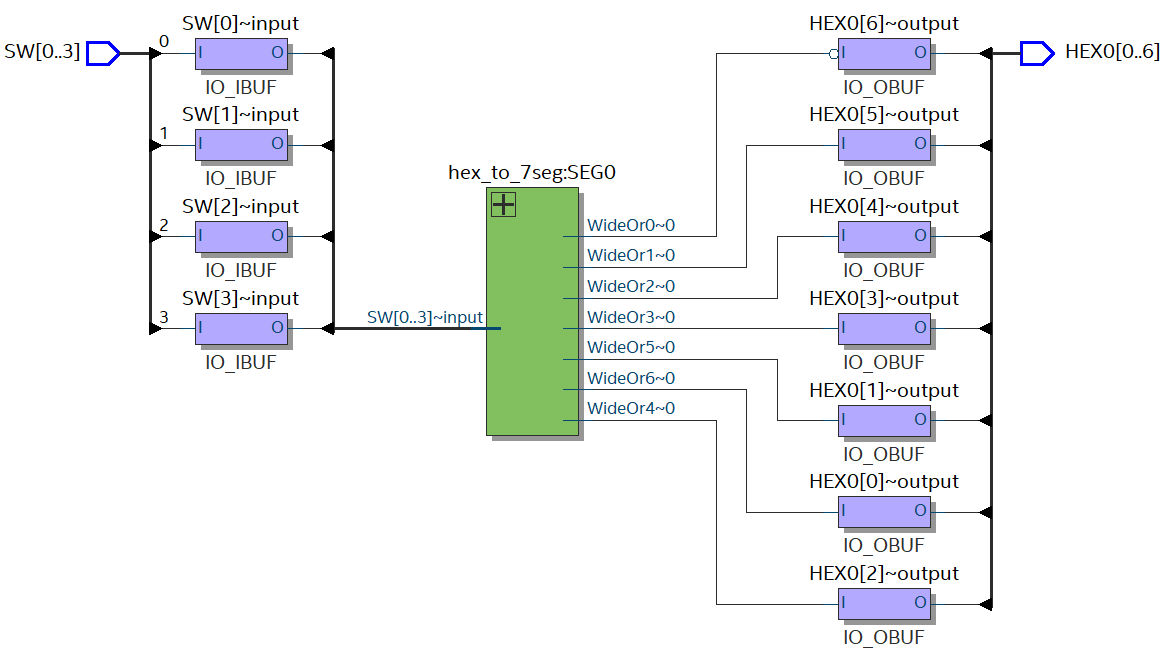
Task 1 Lab report

**Task 2 - Explore Netlist Viewer and Timing Analyzer**

 **Explain what you find and link this back to the Compilation Report.**

* **4 bit binary input is expanded into *OUT[15:0]* for some reason**
* The decode logic implemented with case statements in the Verilog file is converted into a series of *OR* gate, each corresponding to a segment of the 7-segment LED

**Technology Map Viewer (Post mapping)**

* Shows the individual bits of the input and the output
* Shows which output of the *hex\_to\_7seg* links to which output bits